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Notice of Allowability	Application No.	Applicant(s)	
	10/733,626	LIN, CHI-HUI	
	Examiner	Art Unit	•
	David Nhu	2818	
The MAILING DATE of this communication appeal All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication IGHTS. This application is subject to	olication. If not include will be mailed in due	ed course. THIS
1. X This communication is responsive to 7/3/05.			
2. ⊠ The allowed claim(s) is/are <u>14-37</u> .			
3. \boxtimes The drawings filed on <u>11 December 2003</u> are accepted by	the Examiner.		
4. Acknowledgment is made of a claim for foreign priority unal	e been received. be been received in Application No cuments have been received in this is of this communication to file a reply IENT of this application. iitted. Note the attached EXAMINER' es reason(s) why the oath or declarate be submitted. Son's Patent Drawing Review (PTO- S Amendment / Comment or in the CO .84(c)) should be written on the drawing the header according to 37 CFR 1.121(co	national stage applicational stage application of the front (not the d).	quirements IOTICE OF
attached Examiner's comment regarding REQUIREMENT	FOR THE DEPOSIT OF BIOLOGICA	AL MATERIAL.	
Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date	8. ⊠ Examiner's Stateme 9. □ Other	(PTO-413), le nent/Comment	

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REASONS FOR ALLOWANCE

2. Claims 14-37 are allowed.

3. The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggests as cited in claims 14: forming a plurality of parallel long trnches along a first direction in the substrate; forming a conductive layer and a pair of source regions on a bottom of each long trench, wherein the source regions are respectively disposed in the substrate adjacent to two sidewalls of each long trench and electrically connected to the conductive layer; forming source isolation layer on each conductive layer; forming a tunnel oxide layer on two sidewalls of each long trench, contacting the source region thereby; forming a pair floating gates on the source isolation layer, respectively contacting the tunnel oxide layer; forming a pair of inter-gate dielectric layers, respectively overlying the floating gate; forming a pair of control gates, respectively overlying the inter-gate dielectric layer; forming an insulating layer in each long trench, isolating the control gates.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Lin et al (6,093,606): Method of Manufacture of Vertical Stacked Gate Flash Memory Device.

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6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM.

The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu

July 20, 2005

DAVID NHU